REMARKS

Claims 1-29 were pending in this application.

Claims 1-4, 9, 10, 17, 18, 23, and 24 have been rejected.

Claims 5-8, 11-16, 19-22, and 25-29 have been objected to.

Claims 1, 2, 4, 6-12, 14, 15, 17, 20, 21, 23, 24, and 26-28 have been amended as shown above.

Claims 1-29 remain pending in this application.

Reconsideration and full allowance of Claims 1-29 are respectfully requested.

I. ALLOWABLE CLAIMS

The Applicant thanks the Examiner for the indication that Claims 5-8, 11-16, 19-22, and 25-29 would be allowable if rewritten in independent form to incorporate the elements of their respective base claims and any intervening claims. Because the Applicant believes that the remaining claims in this application are allowable, the Applicant has not rewritten Claims 5-8, 11-16, 19-22, and 25-29 in independent form.

II. REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 1-4, 17, 18, 23, and 24 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,810,084 to Jun et al. ("*Jun*"). This rejection is respectfully traversed.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every

element of the claimed invention is identically shown in that single reference, arranged as they are in the claims. (*MPEP § 2131; In re Bond, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)*). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. (*MPEP § 2131; In re Donohue, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985)*).

Jun recites a system where null packets in digital television broadcasting data frames are replaced with training sync signals. (*Abstract*). A null packet detector 120 detects a null packet received in a data format buffer 115. (*Col. 5, Lines 17-18*). When a null packet is detected, the null packet detector 120 stops the operation of a data randomizer 125, a Reed Solomon encoder 130, a data interleaver 135, and a trellis encoder 140. (*Col. 5, Lines 18-23*). The null packet detector 120 also outputs the training sync signals to a multiplexer 145 for transmission to a receiver. (*Col. 5, Lines 18-20*).

Jun lacks any mention of transmitting a "low rate data packet" that includes one or more data bytes each having "information bearing bits and non-information bearing bits" as recited in Claims 1, 17, and 23. *Jun* simply recites that null packets are replaced with training sync signals. *Jun* lacks any mention that the null packets or training sync signals contain one or more bytes, where each byte has "information bearing bits and non-information bearing bits." As a result, *Jun* fails to anticipate all elements of Claims 1, 17, and 23.

For these reasons, *Jun* fails to anticipate the Applicant's invention as recited in Claims 1, 17, and 23 (and their dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 102 rejection and full allowance of Claims 1-4, 17, 18, 23, and 24.

III. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 9 and 10 under 35 U.S.C. § 103(a) as being unpatentable over *Jun* in view of U.S. Patent No. 4,677,625 to Betts et al. ("*Betts*"). This rejection is respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the Applicant to produce evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the Applicant is entitled to grant of a patent. (*In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)*).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or

motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on the Applicant's disclosure. (*MPEP § 2142*).

The Office Action acknowledges that *Jun* fails to disclose a "first data packet switch" and a "second data packet switch" as recited in Claim 9. (*Office Action, Page 4, Last paragraph – Page 5, First paragraph*). The Office Action then asserts that *Betts* discloses these elements of Claim 9 and that it would be obvious to combine *Jun* and *Betts*. (*Office Action, Page 5, First paragraph*).

Betts recites a transmitter that uses multiple trellis encoders 18-24. (*Abstract; Figure 1*). A switching circuit 16 receives four inputs X1-X4 from a randomizer 10 and provides the four inputs to one of the trellis encoders 18-24. (*Col. 2, Lines 30-38*). A second switching circuit 42 receives the outputs from the trellis encoders 18-24 and provides the outputs to a QAM encoder 44. (*Col. 2, Lines 53-62*).

Betts simply recites the use of two switching circuits, a switching circuit 16 providing inputs to four trellis encoders 18-24 and a switching circuit 42 receiving outputs from the four trellis encoders 18-24. None of the switching circuits of *Betts* provides packets to either a "Reed Solomon encoder" or a "data interleaver" as recited in Claim 9. Similarly, none of the switching circuits of *Betts* provides packets to either a "multiplexer" or an "exclusive OR unit" as recited in

Claim 9.

Betts does recite that the trellis encoders 18-24 include XOR gates (*Col. 2, Lines 39-43*). However, the switching circuit 16 only provides the inputs X1-X4 to the trellis encoders 18-24, and the switching circuit 42 only provides the outputs of the trellis encoders 18-24 to the QAM encoder 44. The switching circuits of *Betts* do not provide different kinds of packets to a "multiplexer" and an "exclusive OR unit" as recited in Claim 9.

Moreover, *Jun* cannot be modified by *Betts* to reach the Applicant's claimed invention. For example, *Jun* recites that null packets are detected by the null packet detector 120 and are replaced with training sync signals. The Office Action fails to explain why a switching circuit of *Betts* would be used to send normal packets to the Reed Solomon encoder 130 of *Jun* and to send null packets to the data interleaver 135 of *Jun*. In fact, *Jun* expressly recites that the data interleaver 135 is not used to process null packets (*Col. 5, Lines 18-23*), so a person skilled in the art would not use a switching circuit of *Betts* to provide null packets to the data interleaver 135 of *Jun*.

At most, *Betts* suggests that multiple trellis encoders 140 could be used in *Jun*, and two switching circuits could be used to provide inputs to and receive outputs from the multiple trellis encoders 140. This combination fails to disclose, teach, or suggest a "first data packet switch" that determines "whether a data packet is a full rate data packet or a half rate data packet" and that sends a full rate data packet to a "Reed Solomon encoder" and sends a half rate data packet to a "data interleaver" as recited in Claim 9. This combination also fails to disclose, teach, or suggest a "second data packet switch" that determines "whether a data packet is a full rate data

packet or a half rate data packet" and that sends a full rate data packet to a "multiplexer" and sends a half rate data packet to an "exclusive OR unit" as recited in Claim 9. As a result, the Office Action fails to establish that the proposed *Jun-Betts* combination discloses, teaches, or suggests all elements of Claim 9.

For these reasons, the Office Action fails to establish a *prima facie* case of obviousness against Claim 9 (and its dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 103 rejection and full allowance of Claims 9 and 10.

IV. CONCLUSION

The Applicant respectfully asserts that all pending claims in this application are in condition for allowance and respectfully requests full allowance of the claims.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any fees connected with this communication (including any extension of time fees) or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

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